Low Power Distribution Module for Space Applications: Analysis and Comparison of Different Architectures and DC/DC Topologies

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***Abstract*—The goal of this paper is to analyze and compare different possibilities for the specific design of the DC/DC Power Distribution Module for Space Application. Two architectures and, among them, four well known isolated (Half-Bridge, Push-Pull, Forward with Active Clamp (FWAC) and Flyback with Active Clamp (FLAC)) and nonisolated (Buck and Synchronous Buck) DC/DC topologies are analyzed and compared in terms of efficiency and size, meanwhile taking care of the cost, design time, reliability and flexibility of the whole system. In order to validate presented theoretical results, laboratory prototype for FWAC topology for 28V, 1.75A converter is built and measured. The prototype's minimal 92.3% and maximal 93.2% efficiency match pretty good with expected 92.9% and 94%, respectively.**

I. Introduction

The insertion of power electronics in aerospace technologies is widespread. Solar panels are the primary power source on board of a satellite. When the panels are exposed to the sun they provide power to the load and to charge the on board batteries that are discharged when the satellite is in eclipse. Therefore the satelite main bus is a DC voltage source (Power Bus), which provide few kW of power (down to 100 W for a mini satellite up to 10 kW for a large telecommunication platform). Besides high power electronic unit (for Radar, Electrical Propulsion...) the satellite is plenty of low power multi-output DC/DC converters, which receives the Power Bus and provide a number of different output voltages from 2.2V up to few kV (for scientific instrument devoted to the universe exploration).

Moreover on board of a satellite, DC/DC converters are used to provide power to a number of different loads: digital, analogue, RF with very low noise requirement, scientific instruments and so on.

DC/DC converter building blocks should be designed, not only to improve electrical and manufacturing performances but also to adapt to the different electrical requirements and to mechanically fit in different unit with small non recurring cost.

The above overview leads to the conclusions that flexibility and reliability of the design of DC/DC converters for space application are mandatory.

The goal of this paper is to analyze and compare different possibilities for the design of the DC/DC Power Distribution Module for space application that is supplied from the Main Bus which can operate in the two voltage ranges:

Range 1 - V_{IN} = [45V, 55V]

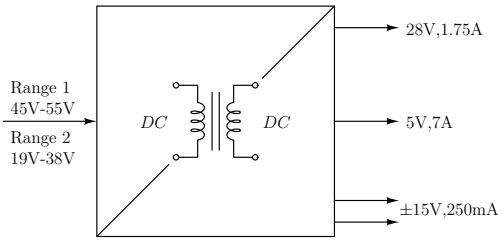

Fig. 1: *Power Distribution Module.*

Range 2 - V_{IN} = [19V, 38V]

and needs to provide four different outputs:

28V, 1.75A
5V, 7A
±15V, 250mA

galvanicaly isolated from the Main Bus. The outputs are not necessary to be galvanicaly isolated between each other. The block diagram of the Power Distribution Module is presented in Figure 1.

In order to cover the both specified operating voltage ranges of the Main Bus (Figure 1), two possible approaches are analyzed and compared:

1) The design of the system that operates in the wide input voltage range V_{IN} = [19V, 60V] that would cover the both operating voltage ranges of the Main Bus
2) The two designs of the system (with minimal differences between each other) that operates in two different input voltage ranges - V_{IN} = [19V, 38V] and V_{IN} = [45V, 55V], which correspond to the operating voltage ranges of the Main Bus.

These two approaches are applied, analyzed and compared to all the architectures and topologies that are proposed in the following sections.

II. Analyzed Architectures

The Architecture A is presented in Figure 2. Its advantages are:

Two converters (Converter 2 and Converter 3) operate in narrow input voltage range, due to the fact that they are supplied from the controlled output of the Converter 1. This can significantly improve efficiency of the system and decrease the design effort for the control, EMI filter and protection circuits. Thus the design time and the total cost of the system could be decreased

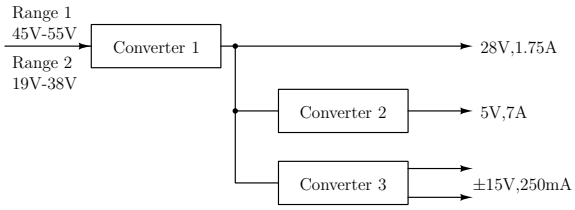

Fig. 2: *Architecture A.*

The Converter 2 is without need for galvanic isolation and thus a simple DC/DC topology can be used for this purpose. This could improve efficiency, cost, weight and reliability of the system

and disadvantages:

The Converter 1 handles full output power of the system, so the size and the weight of this converter can be significantly increased, which can compensate the reduction in the size and the weight of the Converter 2

Flexibility of the system is reduced because failure of the Converter 1 would cause failure of the whole system, even if the two other converters function properly.

The Architecture B is presented in Figure 3. Its advantages are:

All the converters are low power which can decrease the size and the weight of the system

Design time, effort and cost of the system can be significantly improved by adjusting the full design for the one of the converters to the other ones

Flexibility of the system is increased compared to the Architecture A, because the proper function of each of the converters does not depend on the proper function of any other of them

and disadvantages:

All the converters operate in the wide input voltage range, which can increase the design efforts for the control, EMI filter, protection circuits that can increase the total cost of the system

All the converters need to be galvanicaly isolated, which impacts the number of the magnetic components, complexity, cost and size of the system.

III. Analyzed Topologies

Very well known, examined and described in many books and papers ([1] - [5]), galvanicaly isolated topologies:

Half-Bridge

Push-Pull

Forward with Active Clamp (FWAC)

Flyback with Active Clamp (FLAC)

are considered as possible choices for the Converter 1 of the Architecture A (Figure 2) and the Converters 1 and 2 of the Architecture B (Figure 3).

In order to improve efficiency of the system, but without increasing complexity of the driving circuitry nor adding any auxiliary windings to the transformers, possibility of use of self-driven synchronous rectification in the secondary side is also analyzed. As it is already known, FWAC is the only

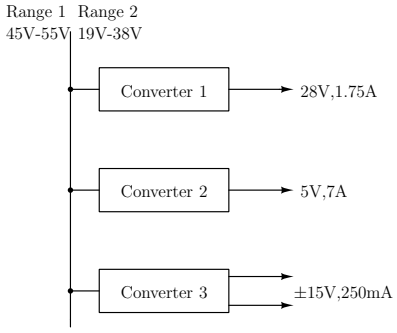

Fig. 3: *Architecture B.*

TABLE I: *Turns Ratios of the HBCC and FWAC topologies presented in order to check the possibility of use of the self-driven synchronous rectification.*

	HBCC	FWAC
$V_{OUT} = 28V$	3.5	2.5
$V_{OUT} = 5V$	0.6	0.4

TABLE II: *Half-Bridge with Complementary Control - Self-Driven Synchronous Rectification.*

HBCC V_{OUT}	Range	v_{GS1min}	v_{GS1max}	v_{GS2min}	v_{GS2max}
28 V	Wide	30.2 V	40.1 V	92.9 V	390 V
	Short	31.8 V	40.1 V	92.9 V	234.1 V
5 V	Wide	5.4 V	7.4 V	15.4 V	66.6 V
	Short	5.7 V	7.4 V	15.4 V	39.9 V

TABLE III: *Forward with Active Clamp - Self-Driven Synchronous Rectification.*

FWAC V_{OUT}	Range	v_{GS1min}	v_{GS1max}	v_{GS2min}	v_{GS2max}
28 V	Wide	47.5 V	150 V	34.4 V	68.2 V
	Short	47.5 V	95 V	39.7 V	68.2 V
5 V	Wide	7.6 V	24 V	6.3 V	14.6 V
	Short	7.6 V	15.2 V	7.5 V	14.6 V

of the topologies mentioned above that allows the use of this approach. Half-Bridge topology, driven in Complementary Control Mode, HBCC [7], also makes this approach possible. Introducing Complementary Control Mode in Half-Bridge topology also reveals the possibility of obtaining ZVS in primary side switches.

A proper self-driven synchronous rectification at the secondary side would be obtained if v_{GS} voltages are in the range [10V, 15V], in order to keep the MOSFET in the ON-state continuously and with the lowest possible R_{DSon} and to be bellow the breakdown v_{GS} with applied deratings (75%).

The results of v_{GS} calculations are presented in Tables II and III, considering the turns ratios listed in Table I. According to these results and aforementioned constraints, self-driven synchronous rectification is impossible to be achieved in any of the cases.

Buck and Synchronous Buck are very well known topologies that are considered as possible solutions for the Converter 2 in the Architecture A (Figure 2).

Flyback with two outputs, as a simplest implementation of multioutput power supply, low power converter, is considered directly, without any comparison with any other topology, as a most appropriate choice for the Converter 3 in both of the

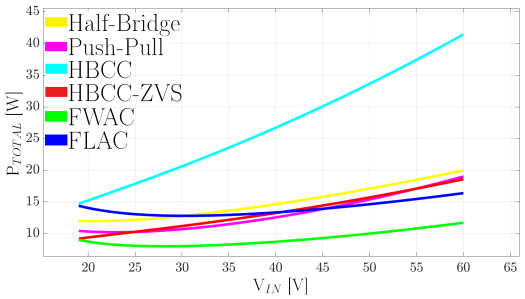

Fig. 4: *Architecture A, Converter 1 (V_{OUT} = 28V, I_{OUT} = 1.75A), V_{IN} = [19V, 60V] - Semiconductor Losses Comparison.*

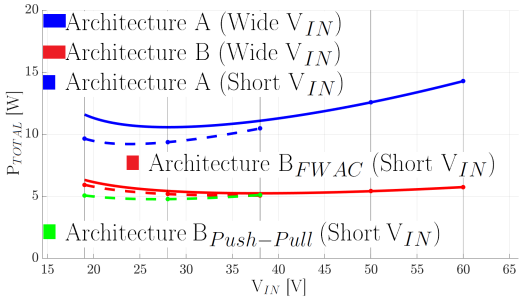

Fig. 5: *Comparison of the Architectures - Semiconductor Losses.*

TABLE IV: *The Choice of the Topologies for the Architectures Comparison.*

	Conv. 1		Conv. 2	
V_{IN} [V]	[19, 60]	[19, 38]	[19, 60]	[19, 38]
Arch. A	FWAC	FWAC	Sync. Buck	Sync. Buck
Arch. B	FWAC	FWAC	FWAC	FWAC/Push-Pull

Architectures. So the comparison of the Architectures will include only comparison of designs of the Converter 1 and the Converter 2. Results of the comparison in terms of losses and size are presented in the following section.

IV. Results of the Comparison

Comparison of the topologies, in terms of semiconductor losses is done for the Converter 1 and the Converter 2 in both architectures and both analyzed input voltage ranges. Applied semiconductor losses model is presented in details in [8], and final equations are listed below:

MOSFET Conduction Losses:
$P_{CM} = R_{DS_{on}} I^2_{D_{rms}}$, where $R_{DS_{on}}$ and $I_{D_{rms}}$ are MOSFET's on-resistance and RMS value of drain current, respectively.
Diode Conduction Losses:
$P_{CD} = u_{D0} I_{F_{av}} + R_D I^2_{F_{rms}}$, where u_{D0}, R_D, $I_{F_{av}}$ and $I_{F_{rms}}$ are diode's on-state zero-current voltage, on-state resistance, average and RMS values of forward current, respectively.
MOSFET Switching Losses:
$P_{SW_M} = (E_{on_M} + E_{off_M})\, f_{sw}$, where

$$E_{on_M} = V_{DS} I_{D_{on}} \frac{t_{ri} + t_{fu}}{2} + Q_{rr} V_{DS} \text{ and}$$

$E_{off_M} = V_{DS} I_{D_{off}} \dfrac{t_{ru} + t_{fi}}{2}$ are MOSFET's turn-on and turn-off energy losses, respectively. V_{DS} is drain to source voltage in the moment of starting/ending switching (turning-on/off) transient, $I_{D_{on}}$ is drain current at the end of turn-on transient, t_{ri} is rise time of drain current, t_{fu} is fall time of drain to source voltage, $I_{D_{off}}$ is drain current in the moment of starting turn-off transient, t_{fi} is fall time of drain current, t_{ru} is rise time of drain to source voltage, Q_{rr} is reverse recovery charge of MOSFET's antiparallel diode and f_{sw} is switching frequency.

Diode Switching Losses:
$P_{SW_D} = (E_{on_D} + E_{off_D})\, f_{sw} \approx E_{off_D} f_{sw}$, where $E_{off_D} = 0.25 Q_{rr} V_{D_{rr}}$ are diode's reverse recovery losses. Q_{rr} and $V_{D_{rr}}$ are diode's reverse recovery charge and voltage during the turn-off transient, respectively. f_{sw} is switching frequency. Diode's turn-on losses, E_{on_D}, are neglected (soft switching-on of diode).

The comparison is given in details in [10] and its example for the Converter 1 of the Architecture A in wide input voltage range is shown in Figure 4. According to the results of this analysis it is decided to compare the architectures considering the choice of the most efficient topologies that is shown in Table IV. Results of the comparison are displayed in Figure 5. The designs' losses for the V_{IN} = [19V, 60V] range differs from 5W up to 8W in favour of the Architecture B. The designs' losses for the V_{IN} = [19V, 38V] range differs from 4W up to 5.5W in favour of the Architecture B with FWAC topology as the Converter 2 and from 4.5W up to 5.5W in favour of the Architecture B with Push-Pull topology as the Converter 2. Difference in losses of 4W up to 5.5W for such a low power DC/DC topologies (49W, 35W, 2X3.75W outputs) can not be compensated by the additional analysis and calculations of magnetic losses, neither by eventual difference in losses for two-output Flyback topology which is considered as the Converter 3 for both of the architectures. Beside this, the Architecture B shows minor variation of the losses in the whole input voltage range, for both V_{IN} = [19V, 38V] and V_{IN} = [19V, 60V]. According to these results, the Architecture B is chosen as more appropriate one to be analyzed further.

Further analysis considers magnetics design for the Converter 1 (FWAC, Push-Pull and FLAC topologies) and the Converter 2 (FWAC and Push-Pull topologies) of the Architecture B. Magnetics designs are provided using the PEmag and PExprt software tools. AC resistances of the magnetics' windings are obtained numerically (Finite Element Analysis - FEA) by the PEmag 2-D modelling which takes into account skin, gap and proximity effects. Magnetics' winding losses are calculated as:

$$P_W = R_{DC} I^2_{DC} + \sum_{k=1}^{n} R_{AC_k} I^2_{RMS_k},$$

where R_{DC} is DC resistance, R_{AC_k} is k-th harmonic's AC resistance, I_{DC} is DC value of the current and I_{RMS_k} is k-th current's harmonic of the corresponding winding. Magnetics'

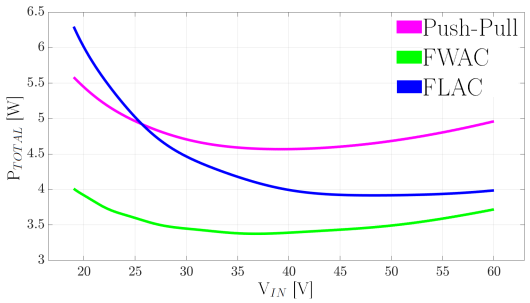

Fig. 6: *Architecture B, Converter 1 (V_{OUT} = 28V, I_{OUT} = 1.75A), V_{IN} = [19V, 60V] - Total Losses (Semiconductor and Magnetic) Comparison.*

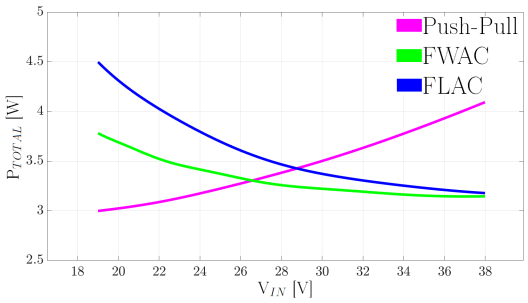

Fig. 7: *Architecture B, Converter 1 (V_{OUT} = 28V, I_{OUT} = 1.75A), V_{IN} = [19V, 38V] - Total Losses (Semiconductor and Magnetic) Comparison.*

core losses are calculated by the Modified *Steinmetz* Equation [9]:

$$P\left[\frac{W}{m^3}\right] = k f_{eq}^{\alpha\ 1} \left(\frac{\Delta B}{2}\right)^{\beta} f_{sw},$$

where P is power density of core losses, ΔB is *peak-peak* variation of flux density, k, α and β are *Steinmetz* coefficients of the magnetic core material and f_{eq} is calculated as:

$$f_{eq} = \frac{2}{(\pi \Delta B)^2} \int_0^T \left(\frac{dB}{dt}\right)^2 dt.$$

Total losses comparison of the selected topologies for the Converter 1 of the Architecture B and the wide input voltage range is shown in Figure 6. FWAC is the most efficient topology in the whole V_{IN} range. Push-Pull has from 1.25W up to 1.5W (2.15% up to 2.54% less efficient) more losses than FWAC. FLAC has from 0.25W up to 2.25W (0.44% up to 3.76% less efficient) more losses than FWAC. FWAC also has the most flat losses characteristic in the whole range, losses varies from 3.4W up to 4W. Push-Pull losses varies from 5W up to 5.6W, while FLAC has the biggest variation of losses, from 4W up to 6.3W. FWAC and Push-Pull have the same size of the transformer (RM8 core) and inductor (RM8/I core), while FLAC least achievable size of the transformer is RM12/I core.

Total losses comparison for the short input voltage range is shown in Figure 7. FLAC topology has the highest maximum point of total losses (4.5W) and the biggest variation of the losses characteristic, from 3.2W up to 4.5W. Losses characteristics of FWAC and Push-Pull topologies cross at V_{IN} = 26.5V. Bellow this point, Push-Pull is more efficient, and over this point, where is the nominal operating point of the converter for the short input voltage range, V_{IN} = 28V, FWAC is more efficient. This advantage is minor - at V_{IN} = 28V FWAC is 0.2% more efficient. Push-Pull topology has higher maximum losses point, 4.1W at V_{IN} = 38V, comparing to 3.75W at V_{IN} = 19V for FWAC topology. Also, FWAC losses characteristic is more flat - 3.2W up to 3.75W losses variation, comparing to 3W up to 4.1W of Push-Pull. FWAC and Push-Pull have the same transformer (RM8) and inductor (RM8/I) size, while FLAC least achievable size of the transformer is RM12/I core.

Total losses comparison of the selected topologies for the Converter 2 of the Architecture B and the wide input voltage range is shown in Figure 8. Losses difference of 0.5W in favour of FWAC topology is almost constant in the whole input voltage range. Variation of the losses characteristic for FWAC topology is from 3.7W up to 4.2W and for Push-Pull topology is from 4.15W up to 4.75W. Size of the magnetics is the same, RM8 core transformers and RM8/I core inductors for both topologies.

Total losses comparison for the short input voltage range is shown in Figure 9. In most of the range, V_{IN} = [19V, 36V], Push-Pull topology is more efficient - up to 1W (2.38% of the efficiency) less losses. In short part of the range, V_{IN} = [36V, 38V], FWAC shows minor advantage, up to 0.1W (0.24% of the efficiency) less losses. Size of the magnetics are the same for both converters, RM8 core size transformer and RM8/I core size inductor.

According to the previous analysis, FLAC topology is discarded as a possible solution for several reasons:

> This topology shows the biggest peak value (6.3W in wide and 4.5W in short V_{IN} range) and has the biggest variations of losses for the both analyzed input voltage ranges.
>
> As it is documented in [10], it is comparable in terms of efficiency with other two topologies only for the case of the Converter 1 of the Architecture B and, like that it is not considered in the comparison for the Converter 2. As it does not show any significant advantage over FWAC and Push-Pull in case of the Converter 1, there is no sense to design different topologies for the Converter 1 and Converter 2 and in that way to increase cost, design time and complexity of the whole system.
>
> Last, but not the least is the practical constraint that size of the RM cores bigger than RM10 was not available for this particular purpose.

As it is already mentioned, for sake of simplicity, cost and design time, it is desirable to have same topology for the Converter 1 and 2. It is also clear that for both, Converter 1 and 2, for wide V_{IN} range, FWAC shows the best results in terms of efficiency, but there is no clear decision on the topology for short V_{IN} range. Thus the final conclusion depends also on the selection of the operating V_{IN} range, that is discussed in Section I.

It would be interesting to analyze the influence of the

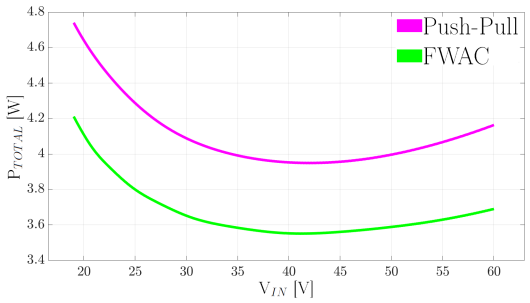

Fig. 8: *Architecture B, Converter 2 (V_{OUT} = 5V, I_{OUT} = 7A), V_{IN} = [19V, 60V] - Total Losses (Semiconductor and Magnetic) Comparison.*

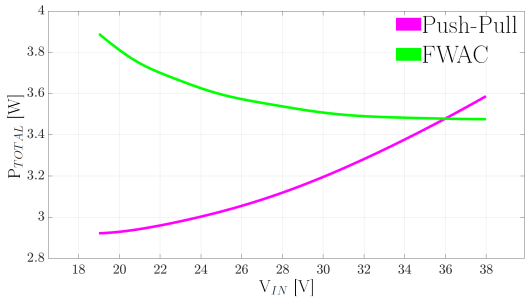

Fig. 9: *Architecture B, Converter 2 (V_{OUT} = 5V, I_{OUT} = 7A), V_{IN} = [19V, 38V] - Total Losses (Semiconductor and Magnetic) Comparison.*

specific design for short V_{IN} range on the efficiency of FWAC topology, as obviously most efficient one in the wide V_{IN} range (Figures 6 and 8). Results of this comparison are displayed in Figures 10 and 11. One can notice that the design for short V_{IN} range has constantly 0.6W advantage for the Converter 1 and up to 0.3W less losses (0.68% more efficiency) for the Converter 2. These advantages can be considered as minor in comparison of having a single design for wide V_{IN} range that can cover both specified operating ranges of the Main Bus (Section I). However, as the dynamics demands and security margins for Space Applications are very severe and hard to fulfill, the wide V_{IN} range can influence a lot of troubles in the design of the EMI filter, control and protection circuitry that are not taken into account in the comparison. These difficulties and their impact on the final design (efficiency, size, cost, design time) are described in details in [11]. Thus the additional analysis of the system's dynamics is necessary for more clear view on this issue, which is beyond the scope of this document and will be the subject of the future work.

All the losses calculations, magnetics designs and comparison are described in detail in [10] and done for the fixed f_s = 100kHz switching frequency.

V. Experimental Results

In order to validate the methodology and theoretical results of the comparison presented in the previous section, FWAC prototype for the Converter 1 (V_{OUT} = 28V) of the Architecture B is built and measured. Power stage of FWAC topology is presented in Figure 12. Fundamental characteristics of the

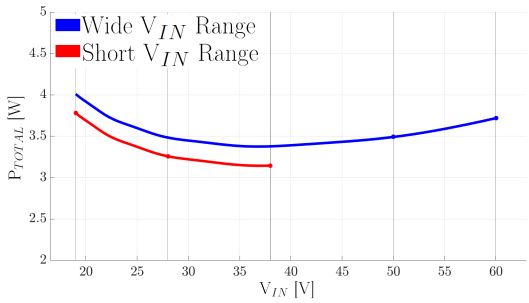

Fig. 10: *FWAC, Architecture B, Converter 1 (V_{OUT} = 28V, I_{OUT} = 1.75A) - Total Losses (Semiconductor and Magnetic) Comparison Between Operating V_{IN} Ranges.*

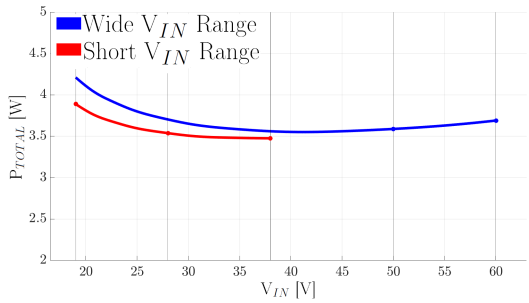

Fig. 11: *FWAC, Architecture B, Converter 2 (V_{OUT} = 5V, I_{OUT} = 7A) - Total Losses (Semiconductor and Magnetic) Comparison Between Operating V_{IN} Ranges.*

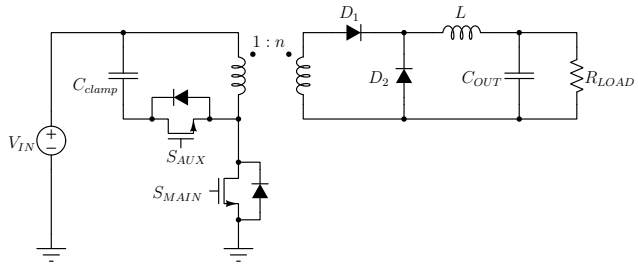

Fig. 12: *Power Stage of FWAC Converter.*

prototype's design and selected components are sumarized in Table V. It should be mentioned that because of the cost, Rad-Hard (Radiation Hardened) semiconductor devices, that are used in Space Applications, are replaced by the standard industrial equivalent semiconductors that fit them best in terms of losses. Main waveforms at V_{IN} = 28V, I_{OUT} = 1.75A, that validate the proper function of the prototype, are shown in Figure 13.

Theoretical and measured results for losses and efficiency are provided in Figure 14. One can notice that the chosen industrial equivalents show negligible difference in losses comparing to the Rad-Hard devices, which means that the experimental validation is fair. On the other hand, measured losses are higher from 0.35W up to 0.5W than it was predicted, which means that instead of the expecetd minimal 92.9% and maximal 94% efficiency, the prototype reaches 92.3% and 93.2%, respectively. Comparing this deviation with the values from the previous sections, it can be assumed that there is no significant influence of it on the final conclusions that can be based on the presented theoretical results.

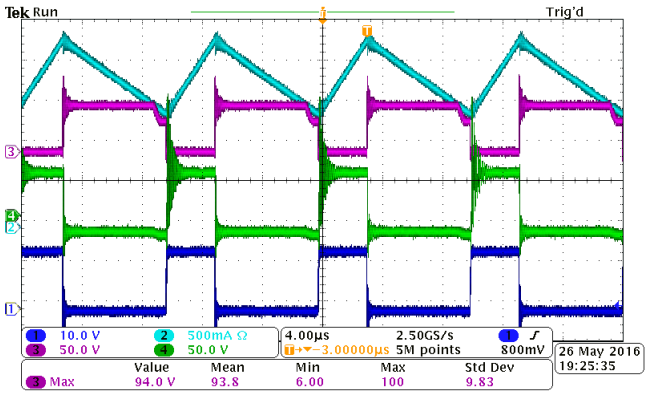

Fig. 13: *FWAC, Architecture B, Converter 1 ($V_{OUT} = 28V$), V_{IN} = [19V, 38V] - Prototype Waveforms at $V_{IN} = 28V$, $I_{OUT} = 1.75A$ (i_L, $v_{DS_{MAIN}}$, $v_{DIODE_{(1-D)}}$, $v_{GS_{MAIN}}$).*

TABLE V: *FWAC, Architecture B, Converter 1 ($V_{OUT} = 28V$), V_{IN} = [19V, 38V] - Design of the Prototype.*

Semiconductors	Rad-Hard	Ind. Equiv.
Main MOSFET	IRHYK57133CMSE	IRFB23N15DPbF
Aux. MOSFET	IRHYK57133CMSE	IRFB23N15DPbF
DIODE D_1	60LQ100	VS-60CTQ150PbF
DIODE D_2	75LQ150	VS-60CTQ150PbF
Core Design	Transformer	Inductor
Manufacturer	Epcos	Ferroxcube
Core Size	RM8	RM8/I
Core Material	N97	3C95
Gap [mm]	//	0.42
L_m [μH]	324.37	187.86
Windings Design	Transformer	Inductor
	Prim. / Sec.	
Number of Turns	10 / 25	29
Wires in Parallel	4 / 2	3
Wire Size	AWG26 / AWG26	AWG26
Wire Diam. [mm]	0.4 / 0.4	0.4
Wire Length [mm]	273.18 / 682.95	792.22
DC Res.	15.35 $m\Omega$ / 99.31 $m\Omega$	66.56 $m\Omega$
AC Res. (@f_{SW})	37.45 $m\Omega$ / 220 $m\Omega$	380 $m\Omega$

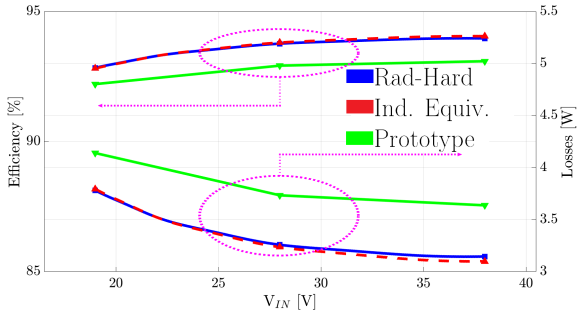

Fig. 14: *FWAC, Architecture B, Converter 1 ($V_{OUT} = 28V$), V_{IN} = [19V, 38V] - Comparison of the Calculations and the Prototype Measurements at $I_{OUT} = 1.75A$.*

VI. Conclusions and Future Work

The goal of this paper was to analyze and compare different possibilities for the specific design of the DC/DC Power Distribution Module for Space Application. Two operating input voltage ranges, two architectures and, among them, several well known isolated and nonisolated DC/DC topologies are analyzed and compared in terms of efficiency and size, meanwhile taking care of the cost, design time, reliability and flexibility of the whole system.

According to the results of the comparison based only on semiconductor losses, the Architecture B, that is consisted of three low power converters connected directly to the Main Bus (Figure 3), was the obvious selection for the further analysis. These results were also considered as sufficient for discarding some of the topologies, so magnetics are designed for FWAC, FLAC and Push-Pull topologies for the purpose of further examination. FWAC topology shows the best efficiency for the design of both, the Converter 1 and 2, for wide V_{IN} range. Design of the FWAC topology for short V_{IN} range shows minor improvement in the efficiency (up to 0.68%), comparing to the possibility of having the single design of the system that can cover both operating voltage ranges of the Main Bus.

As there is no clear conclusion on the topology for the short V_{IN} range design, neither the conclusion on the operating input voltage range, the additional analysis of the system's dynamics is considered as a subject of the future work in order to have more clear view on these issues.

Laboratory prototype for FWAC topology for the Converter 1 ($V_{OUT} = 28V$) of the Architecture B is built and measured in order to validate the presented theoretical analysis. The prototype's minimal 92.3% and maximal 93.2% efficiency match pretty good with expected 92.9% and 94%, respectively.

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